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10 bit Delta Sigma D/A Converter with Increased S/N ratio Using Compact Adder Circuits

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Abstract— Data converters, ADCs and DACs, interface the real world of analog signals to the digital domain. They can be classified as 'Nyquist rate converters' and 'Over sampled converters'. Former operates at a sampling rate of twice the input signal frequency. They do not make use of the advantages of exceptional high speeds achieved in the current VLSI technology. Also the limitations in matching accuracy of the analog circuits needed in this type, limits their accuracy to an effective number of bits (ENOB) of 12 to 14 bits for various implementations. Over sampling data converters uses sampling rate much higher than Nyquist rate, typically higher by a factor between 8 and 512 or higher. They can achieve over 20 ENOB resolution at reasonably high conversion speeds. The engine behind this over sampling converter is a delta-sigma modulator. The main advantage of delta sigma modulator is that they offer a very good separation of input signal from the quantisation noise due to the over sampling process and noise shaping. The Signal to noise ratio (SNR) for a Nyquist rate converter depends on the number of bits of the converter. In this type SNR can be increased by approximately 6dB per bit. In over sampling converters the SNR depends on the depth of oversampling also, which is specified as 'Oversampling ratio' (OSR). Theoretically, for each doubling in sampling rate SNR can be be improved by a factor of 3dB, , which corresponds to a half bit increment in Nyquist rate converters. Thus without increasing chip area SNR is increased. In this paper a 10 bit delta sigma DAC is implemented and SNR was measured with various sinusoids at different over sampling ratios. To reduce the number of transistors in the implementation, 'Minimal energy dual bit adder (MEDB adder) is used.

Index Terms— Data converter, delta-sigma modulator, over sampling, noise shaping, delta-sigma data converter; effective number of bits.

1 Introduction

MOST signals in nature are analogue, representing continuous variations of physical quantities, in time or space. The processing of these signals is more effectively done in digital domain with high accuracy. Digital circuits are robust and can be realized by extremely small and simple structures, which can in turn be combined to obtain very complex, accurate and fast systems. So computational and signal processing tasks are now performed predominantly by digital means. The digital processing techniques have the advantage of high accuracy, lossless and high density storage with perfect reproducibility, low cost and high reliability.

ADCs and DACs, combinely known as data converters, are necessary to interface the real world of analogue signals to the digital system. As the speed and density of the Integrated circuits is increased the speed and accuracy of data converters associated with them should be increased.

2 Procedure for Paper Submission

Data converters can be classified into two main categories. Nyquist rate data converters and Over sampled data converters.

2.1 Nyquist rate Data Converters

Conventional high resolution A/D converters, such as successive approximation and flash type converters, operate at a sampling frequency approximately equal to twice the maximum frequency in the input signal.ie at Nyquist rate. They do not take the advantage of exceptionally high speeds achieved with the current VLSI technology. Also the analog circuitry required in conventional A/D converters limits their accuracy in representing the digital signal. This is due to the limitations in matching accuracy of the analog components like resistors, capacitors, current sources etc. Practical conditions restrict their accuracy to an Effective Number of Bits (ENOB) of 12 to 14 bits for various implementations. For high fidelity applications, such as digital audio, high resolution and linearity is required. An ENOB of 18 or greater is required. Also modern sophisticated signal processing requires dynamic range of operation, which cannot be fully satisfied by the conventional ADCs. Also, in Nyquist rate converters each input sample is separately processed, regardless of the past input samples, ie. there exists a one to one correspondence between the input and output samples. In other words the converter has no memory.

In data converters, the quantization noise greatly affects the quality of the signal. This is quantitatively expressed as the Signal-to-Quantization-Noise Ratio (SQNR),Where SQNR = Signal power / Quantization noise power. If the input signal is large when compared to the quantization step 'Δ' the error term e(n) is a random quantity uniformly distributed in the interval [-Δ/2,Δ/2] [1]. If the values of e(n) are assumed to be uncorrelated and identically distributed, the quantization noise can be assumed as white and its power is spread uniformly over the entire signal band with frequency range [-fs/2, fs/2]. Thus the power spectral density (PSD) of the noise, at the output of the conventional ADC, N(f) can be expressed as $N(f) = \Delta 2 / 12$. A common measure of a converter's accuracy is the signal-to-noise ratio (SNR) for a sine wave input. If the input sine signal has a full scale amplitude variation $2A = (2B – 1)\Delta$, its power is A2/2, then the SQNR of a Nyquist rate converter can be expressed as

$$SQNR = 10\ log\left(\frac{A^2/_2}{\Delta^2/_{12}}\right) = 10\ log\left(\frac{3.2^{2B}}{2}\right)\ dB$$

The above equation can be simplified and approximated as $SQNR = 6.02B + 1.76\ dB$, where 'B' is the no of bits of the converter. Thus, the maximum achieved SQNR and the quantization error depends on the number of bits B used to represent the samples. In other words, if the number of bits B is incremented by 1bit, the quality of the digital signal, represented by the SQNR, increases by 6 dBs [2].

2.2 Over sampling Data converters

Over sampling data converters uses sampling rate much higher than Nyquist rate. The digital circuitry as well as some analog stages required for the implementation of oversampling converters need to be operating at a much higher frequency. However, when compared to those associated with Nyquist rate converters, the accuracy requirements on the analog components are greatly relaxed. Also, it generates each output utilizing all preceding input values. Thus the converter incorporates memory elements in its structure. This property removes the one to one relation between input and output samples. Over sampling data converters are able to achieve over 20 Effective Number of Bits (ENOB) resolution at reasonably high conversion speed. For enhancement in accuracy, faster operation and extra digital circuitry is needed. Both of these are getting cheaper as digital IC technology advances. Hence the over sampling converters are gradually replacing existing dominated Nyquist rate converters.

Oversampling means sampling at a higher rate 'fs' higher than the Nyquist rate 'fN'. The term Oversampling Ratio(OSR) can be used to represent the depth of over- sampling. OSR is the defined as OSR = fs/fN. Its value is usually taken to be a power of 2. If the value of OSR is between 2 and 16 it can be called as mild oversampling and If the value is above 16 then it is called as heavy over-sampling. The result of oversampling approach can be graphically shown as in fig.1 In figure OSR value is chosen to be 4. Images of the signal band are far apart than in the Nyquist rate sampling. As a result, the specifications of the anti-aliasing filter can be relaxed. Moreover, the accuracy of the digital signal, as far as the SQNR is concerned, can be improved by oversampling. This is shown in Fig. 2. When oversampling is used, the quantization noise power is distributed over a larger frequency range. Consequently, the noise power, corresponding to the quantization noise, lying in the signal band is reduced. The quantization noise lying outside the signal band can be eliminated by means of a digital filter. In an over sampling converter with OSR=R and a full scale input sine wave, the SQNR is evaluated in dBs as [3]

$$SNR_{Oversampling} = 10\ log\left(\frac{A^2/_2}{\left(\Delta^2/_{12}\right)/OSR}\right) dB$$

It can be simplified as SQNR = 6.02B+1.76+10log(OSR) dB The above equation shows that if sampling rate is double the Nyquist rate, ie, OSR =2, the SNR will be improved by a factor of 3dB. This is equivalent to adding half a bit in the resolution of the quantizer of a Nyquist rate data converter. As an example, for digitizing audio signals instead of using a Nyquist rate ADC having sampling rate of 44.1 kHz with 12 bit accuracy, an over sampling converter can be used with sampling rate 44.1 X 4 = 176.4 kHz with 11 bit accuracy without much loss in signal quality.

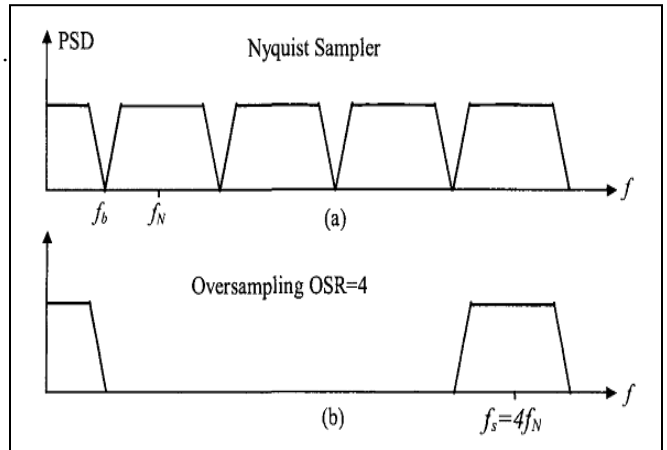

Fig. 1. Graphical representation of over sampling approach. (a) Nyquist rate (b)oversampling

A common measure of a converter's accuracy is the signal-to-noise ratio (SNR) for a sine wave input. The general relationship between Effective Number of Bits (ENOB) and SNR is $SQNR = 6.02B+1.76+10log(OSR)$ dB .The inverse relationship$ENOB = (SQNR - 1.76)/6.02$ is often applied to oversampling converters to convert an SNR to effective number of bits.

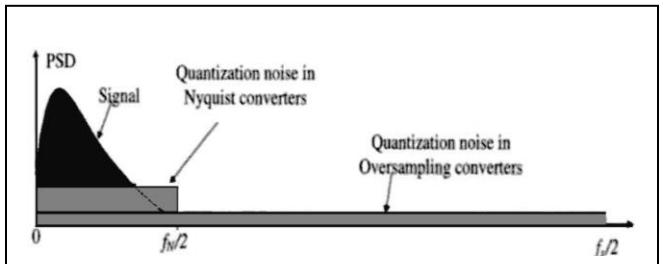

Fig. 2. Quantization noise in Nyquist and oversampling converters

3 Predictive Modulators

When a signal is oversampled, there will not be any significant changes between successive samples, since they are very close. So future samples can be predicted from the past ones since there exist a high correlation between them. Thus, in addition to the improvement in the SQNR, over sampling motivates 'prediction'. In other words, a reduction. in the number of the

quantization levels can be achieved if the difference of two consecutive samples is encoded. A modulator whose operation is based on the prediction principle is called a 'predictive modulator'.

3.1 Delta modulators

Delta Modulator (DM) is the simplest predictive modulator which can be drawn as a simple feedback loop as in fig. 3. Initially it was proposed to convert a low frequency analog signal into a stream of bits which could be easily transferred through noisy channels. As in the block diagram,

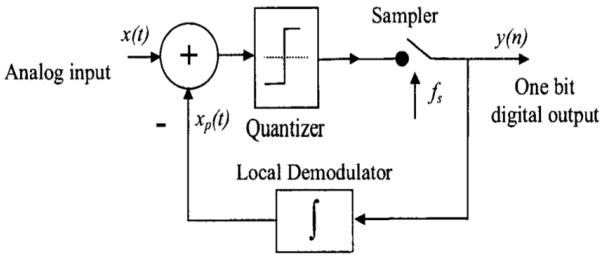

Fig. 3. The Delta Modulator

the sign of the difference between the input and feedback signals is actually encoded as the binary pulse stream 'y(n)', at the output of the Delta modulator, hence the prefix delta. The integrator plays the role of the local decoder so that the feedback signal xp(t) would be always approximating the input analog signal x(t). Thus the decoder circuit at the receiver also should be the exact replica of this . The number of positive or negative pulses at the output bit stream depends on the slope of the input signal and so the the name of the Delta-Modulator. The linear Delta-Modulator is difficult to be analyzed since the quantizer is a non-linear device. Also, slope overload is one of the major drawbacks of Delta modulator, ie. this encoder cannot respond to fast changes of the input signal.

3.1 Delta sigma modulators

If it is possible to push the in-band noise, left after the oversampling, outside the signal frequency band as shown in Fig. 4 further improvement in the SQNR can be achieved. This can be achieved if the signal transfer function STF(z) is all-pass whereas, the noise transfer function NTF(z) is high pass. Improving the SQNR using this technique is called 'noise shaping'. It can be easily and efficiently implemented by modifying the DM system. Here the basic idea is that instead of encoding input signal directly, the integral of the input signal is encoded. Since Integration is a linear function it does not affect the system functionality, whether it is placed at the beginning or at the end of the system. Thus the demodulator integrator (or filter) int the DM can be placed at the input, as it is shown in Fig. 5. For the same reason as above, the two integrators can be replaced by one which is placed inside the DM loop. The significant modification achieved in the DM is that is that matching of the analog integrator and the digital integrator is not required any more, since the same integrator performs both functions. The resulting delta sigma modulator block is shown in fig 6.

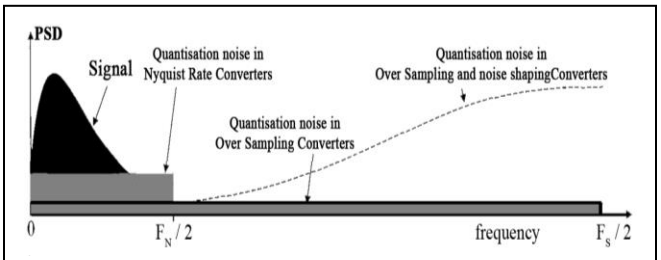

Fig. 4. Spectrum at the output of a noise shaping quantizer.

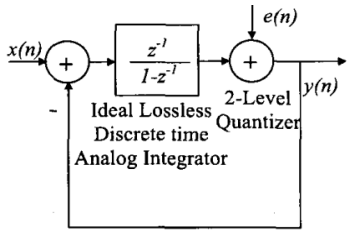

Fig. 5. The two integrators replaced by one placed inside the DM loop

The first-order Delta sigma modulator employs over sampling to spread the quantization noise over the [0, fs/2] frequency band, as well as noise shaping in order to push most of the in-band noise out of this band to higher frequencies. The analysis using Z transform [4] shows that the signal transfer function STF(z) = z-1 leaves the signal unaltered, just delayed by a single bit period. The noise transfer function NTF(z) = 1- z-1 high-passes the quantization

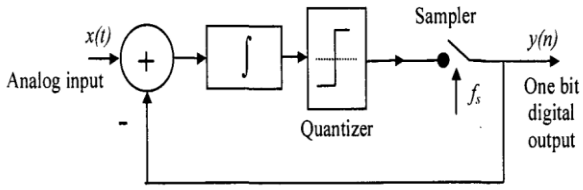

Fig. 6. The Delta Sigma Modulator

error. i.e. it shapes quantization error by suppressing it at low frequencies. As a result, the quantization noise power inside the signal band [0, fs/2R] ≡ [0, fb], with oversampling ratio OSR = R, will be lower than its value when no noise shaping is applied. Oversampling spreads the quantization noise spectrum uniformly over the whole frequency band, thus leaving a small portion of it inside the signal band. Noise shaping, on the other hand, reduces the quantization noise power inside the signal frequency band even further, by pushing most of the in-band noise outside the signal band.

4 PROPOSED ARCHITECTURE

Most of the over sampling data converters are Delta sigma data converters. The delta sigma modulator is the core of delta sigma data converters. it produces a bit-stream. Here in this paper a digital to analog converter based on delta-sigma engine is implemented. Proposed architecture for an N bit Digital to Analog converter based on Delta Sigma Engine [5] is shown in Fig. 7.

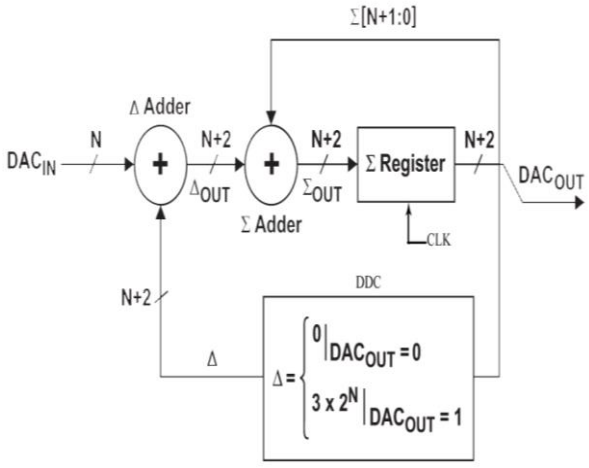

Fig. 7. Proposed DAC architecture

A Delta Sigma DAC makes computations using binary adders. The functionality of the different modules in the architecture is explained below.

4.1 Delta adder and DDC

Delta adder is used to compute the difference between the DAC input and Digital to Digital Converter (DDC) output as in Fig. 7. The Δ feedback signal from DDC to the delta adder depends on the DAC output which is a single bit. It will be either a 1 or a 0. If it is a 0, then DDC out Δ is an N+2 bit number with all 0s. If DAC output is a 1, then Δ is the 1's complement of the highest N bit number, sign-extended to N+2 bits. This is equivalent to two 1s concatenated as MSBs to an N bit number of all 0s. The DACIN is an unsigned number. But, since the outputs of both adders represent signed numbers, it is sign-extended. Therefore, the outputs of the delta adder and sigma adder are signed numbers.

In this implementation, since the DACIN is of 10 bits and the output of the adders will be of 12 bits. When the DAC input is 0, the output is always 0 V. If the DAC output is a 0, then DDC out Δ is 12 bits of all 0s. If DAC output is a 1, then Δ will be a 12 bit binary number with two 1s concatenated as MSBs to 10 bits of zeroes.

4.2 Sigma adder and Sigma register

Sigma adder is used to compute the sum of the delta adder output and the current content of the sigma register. The output of the sigma adder is stored in the sigma register. The MSB of the sigma register is taken as the DAC output (DACOUT). The functionality of the sigma adder is similar to that of an integrator, which accumulates the input at a rate or slope proportional to the magnitude of the input. When the MSB of the Sigma register becomes 1, it becomes a negative number, and the Δ error signal is subtracted from Σ such that the accumulated value is reduced to a smaller positive value. The integration is continued until the next overflow takes place. The MSB of sigma register is the DACOUT, and the rate at which the MSB becomes 1 is directly proportional to the input magnitude. Also, the density of 1s in the DACOUT bit-stream is also directly proportional to the DAC input.

5 IMPLEMENTATION OF BASIC BLOCKS

As in the architecture the main functional blocks are two 12bit adders, a 12bit register and a Digital to Digital Converter (DDC). The size of the DAC input is 10 bit.

5.1 Adder circuits

For implementing 10bit Delta sigma DAC, 12 bit adders are required. In this implementation to reduce the number of transistors [6] compact adder circuit was used. The realised adder circuit is known as MEDB (Minimal energy dual bit adder[7]. Thus the basic block of the adder circuit is a dual bit adder. Six such dual bit adders are cascaded to form 12 bit adders. The circuit diagram of the dual bit adder for S_0 bit, S_1 bit and C_{out} bit is shown. S_0 requires 13 transistors Fig.8, S_1 requires 23 transistors Fig. 9 and C_{out} requires 17 transistors Fig . 10.

5.2 D Flip Flop

The implementation of the 10 bit Delta Sigma DAC architecture requires a 12 bit Sigma Register. The output of a delta sigma data converter is always a stream of pulses. Here the most significant bit of the sigma register forms the actual DACout bit stream. Flip Flops are the basic building blocks of registers. The 12 bit register is implemented from the basic CMOS D Flip-Flop circuit which is realized as a negative edge triggered Master-Slave Flip flop [8]. The over sampled clock pulses are fed at the clock input of the sigma register. Thus the delta sigma DAC generates each output utilizing preceding input values, where the sigma register acts as the memory element. Each single bit Flip flop requires 18 transistors. The circuit diagram is shown in Fig 11.

5.3 Digital to Digital Converter

The Δ feedback signal to the delta adder is fed from DDC. It depends on the DAC output which is a single bit. It will be either a 1 or a 0. As stated previously If it is a 0, then DDC out Δ is a 12 bit binary number with all 0s. If it is a 1, then Δ is the 1's complement of the highest 10 bit number, sign-extended to twelve bits. It is equivalent to two 1s concatenated as MSBs to an N bit number of all 0s.

Thus the functionality of the digital to digital converter can be realized by making proper feedback connections to the delta adder. No extra transistors required for this.

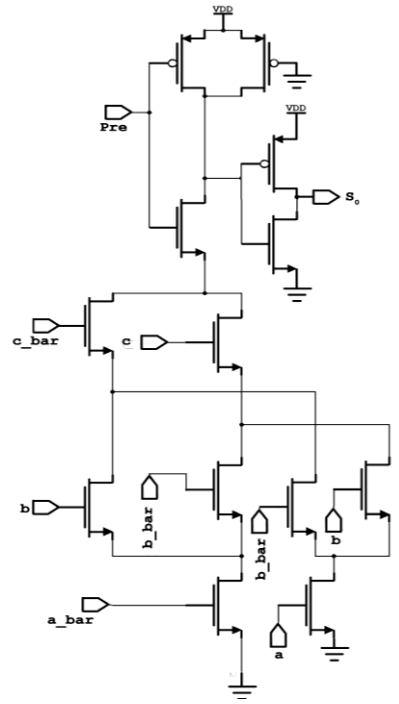

Fig. 8. S_0 bit in the dual bit adder

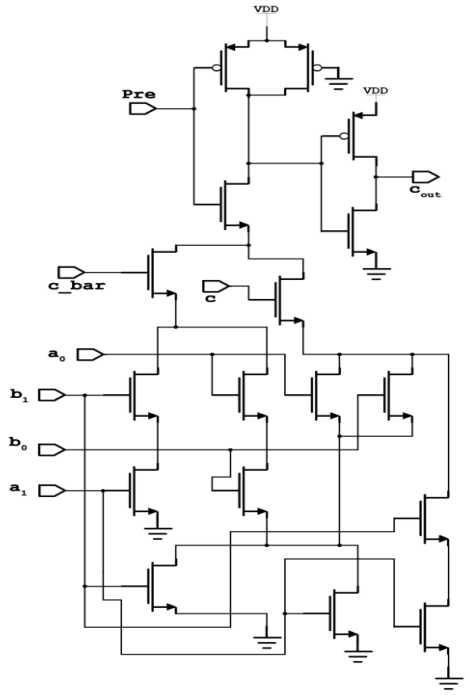

Fig. 10. C_0 bit in the dual bit adder

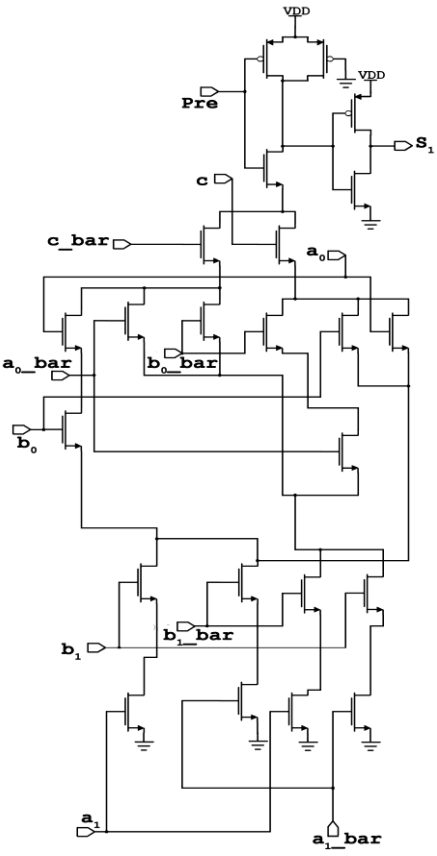

Fig. 9. S1 bit in the dual bit adder

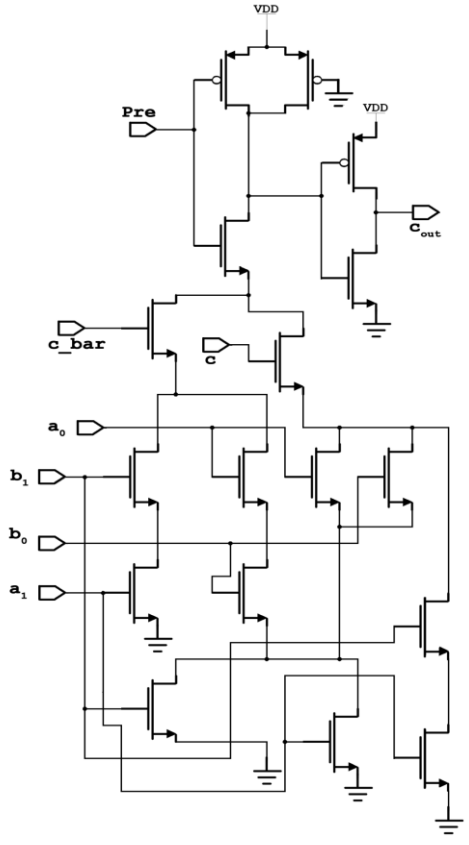

Fig. 11. Negative edge triggered D Flip Flop-single bit.

6 EXPERIMENTAL RESULTS

The simulation was done on Mentor graphics tool kit. The schematic entry was done with Mentor Graphics Design Architect. The Simulation tool used is Mentor Graphics Eldo Spice and the Layout Design tool is Mentor Graphics IC Station. The technology used is TSMC 180nm CMOS Technology. For measuring the SQNR of the 10 bit delta sigma DAC a number of simulations were conducted. Out of them four different simulations were selected here. The input to the DAC was fed from a built in ADC macro module in the schematic library. The outputs of simulations were fed to MATLAB for measuring the obtained SQNR. Each simulation was conducted at different Over sampling ratios. The details are tabulated in table 1. The obtained results are compared with theoretical values.

TABLE 1
MEASURED SQNR RESULTS OBTAINED, COMPARED WITH MAXIMUM THEORETICAL LIMITS

	SQNR Results of 10 bit DAC				
DAC details	***Nyquist rate***	***Implemented 10 bit delta sigma DAC***			
		OSR 8	***OSR 16***	***OSR 32***	***OSR 64***
Maximum Theoretical limit (dB)	61.96	70.99	74.00	77.01	80.02
Obtained SQNR value (dB)	--	70.02	73.07	76.21	79.21

CONCLUSION

The delta sigma based data conversion technique is a cost effective alternative for high resolution data converters. The delta sigma data converters offer a very good separation of input signal from the quantization noise. In the implementation of 10 bit delta sigma DAC compact Minimal Energy Dual Bit adder circuits were used which saves an area up to 24.4% on the adder implementation than normal Carry look ahead adder implementation. The SQNR values obtained were very closer to the theoretical limit. As CMOS technology feature size is continuously decreasing, the delta-sigma converters will operate at higher frequencies and finer resolution at a lower cost.

REFERENCES

[1] R.M Gray, "Quantization Noise Spectra," IEEE Transactions on Information Theory, Vol 36, November 1990.

[2] Gonzalo R. Arce, Nikolai A. Grabowski, Neal C, Gallagher, "Weighted Median Filters with Sigma – Delta Modulation Encoding," IEEE Transactions on Signal Processing, Vol 48, No. 2, Feb 2000.

[3] J.C. Candy,G.C Temes Holmdel, "Oversampling Delta – Sigma Data Converters, IEEE Press, 1991

[4] Shanthi Pavan , "Oversampling Analog-to-Digital Converter Design", VLSID 2008. 21st International Conference , VLSI Design, 2008

[5] Hugo Cheung, MSC Group, Data Acquisition Products, Texas Instruments Incorporated " Implementation of 12 bit delta sigma DAC with MSC12xx Controller"

[6] B.Ramkumar, Harish M.Kittur and P.Mahesh Kannan, "ASIC Implementation of Modified Faster Carry Save Adder", European Journal of Scientific Research, Vol.42, Issue 1,2010.

[7] Obridko,I,.Ginosar ,"Minimal Energy Asynchronous Dynamic Adders", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, , pp. 1043 - 1047 Volume: 14 , Issue: 9,2006

[8] N. Weste and K. Eshraghian , 'Principles of CMOS digital design'.

[9] Pervez M. Aziz, Henrick V. Sorensen, Jan Van Der Spiegel, "An Overview of Sigma Delta Converters" IEEE Signal Processing Magazine, Jan 1996.

[10] Eren Turgay, Aaron Daniels, Michael Bacelieri, William Berry, "CMOS Binary Fulladder, A Survey of Possible Implementations"